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[METHOD FOR FABRICATING A NON-VOLATILE MEMORY AND METAL INTER-CONNECT PROCESS]

Abstract

A method for fabricating a non-volatile memory is provided. A stacked structure including a tunneling layer, a trapping layer, a barrier layer, and a control gate is formed on a substrate. A source region and a drain region are formed beside the stacked structure in the substrate. A silicon oxide spacer is formed on the sidewalls of the stacked structure. An ultraviolet-resistant lining layer is formed on the surfaces of the substrate and the stacked structure to prevent the ultraviolet light from penetrating into the trapping layer. A dielectric layer is formed on the ultraviolet-resistant lining layer. A contact being electrically connected to the control gate is formed in the dielectric layer. A conducting line electrically connected to the contact is formed on the dielectric layer. A low-surface-charge lining layer is formed on the surfaces of the dielectric layer and the conducting line to reduce the antenna effect.